AMENDMENTS TO THE CLAIMS

1.   (Original) A platform comprising:

a processor executing in one of a normal execution mode and an isolated execution mode;

a system memory including an isolated area, an isolated output area, and a non-isolated area; and

an output device.

2.   (Original) The platform of claim 1 wherein the output device is a graphics card.

3.   (Original) The platform of claim 2 further comprising:

a memory control hub (MCH) coupled between the system memory, and the processor and the graphics card, the memory control hub to permit the graphics card to access the isolated output area only when the graphics card is in isolated access mode.

4.   (Original) The platform of claim 3 wherein the graphics card comprises:

a direct memory access (DMA) controller and wherein local storage of the data from the isolated output area is not permitted.

5.   (Original) The platform of claim 3 wherein only the graphics card is permitted to read the isolated output area.

6.   (Original) The platform of claim 1 further comprising:

an operating system (O/S) nub having a driver to write display data into the isolated output area when the processor is executing in isolated execution mode.

7.   (Original) The platform of claim 3 further comprising:

a link between the graphics card and the MCH having an isolated transaction type.

8. (Original) The platform of claim 3 wherein the MCH only permits the O/S nub to write to the isolated output area.

9. (Original) The platform of claim 7 wherein the link is a secure accelerated graphics port bus.

10. (Original) The platform of claim 2 wherein the graphics card comprises:

an isolated bit plane; and

a non-isolated bit plane.

11. (Original) The platform of claim 10 wherein the graphics card denies all external access to the isolated bit plane.

12. (Original) A method comprising:

establishing an isolated execution environment having an isolated execution mode; and

preventing access to output data by any requester not operating in an isolated mode.

13. (Original) The method of claim 12 wherein establishing comprises:

segregating a system memory into an isolated output area and a non-isolated area.

14. (Original) The method of claim 13 further comprising:

issuing an isolated direct memory access (DMA) request for display data in the isolated output area from a graphics card; and

refreshing the display based on the display data.

15. (Original) The method of claim 13 wherein preventing comprises:

identifying if an isolated attribute is present in a request for access to the isolated output area; and

denying the request if no isolated attribute is present.

16. (Original) The method of claim 13 further comprising:

loading data from the isolated output area into a bit plane on a graphics card; and

denying all external access to the bit plane.

17.   (Original) The method of claim 16 further comprising:

defining a first window for display of an image corresponding to the bit plane; and

occluding all windows but the first window.

18.   (Original) The method of claim 13 further comprising:

retrieving data from the isolated output area;

displaying an image corresponding to the data; and

occluding the image prior to a platform transitioning out of isolated execution mode.

19.   (Original) A platform comprising:

a processor executing in one of a normal execution mode and an isolated execution mode;

a direct memory access (DMA) controller to issue requests for access to an isolated output

area;

a first interface coupled to the DMA controller to forward requests to a memory control hub

(MCH); and

a second interface coupled to the DMA controller to supply output data to an output device.

20.   (Original) The apparatus of claim 19 wherein the first interface is a secure accelerated

graphics port (AGP) and the output device is a display.

21.   (Original) The apparatus of claim 19 wherein the DMA controller attaches an isolated

attribute to any isolated output area access request.

22.   (Original) The apparatus of claim 19 wherein the second interface is an audio interface.